REMARKS

This is in response to a final Office Action mailed August 4, 2003. In the present final Office Action, claims 2, 4-11, 13, 17-19, 21 and 22 currently stand rejected. Applicant respectfully traverses and requests reconsideration.

Applicant respectfully submits the above proposed amendments do not provide for any new subject matter. Furthermore, Applicant respectfully requests the Examiner to enter the above amendments and submit that these amendments are not narrowing in nature nor do they require the Examiner to conduct any further prior art searching as these limitations amended to claims 21 and 22 have been previously presented as previously pending claims 4 and 19, respectively. Therefore, it is submitted the Examiner does not have to conduct any further searching and the amendments do not add any new matter. As such, entrance of the above amendments is respectfully requested by the Examiner for the furtherance of the present prosecution of this application and the passage of these claims to issuance.

Rejection of claim 21 under 35 U.S.C. §102(b)

Claim 21 currently stands rejected under 35 U.S.C. §102(b) as being anticipated by Noble et al., U.S. Patent No. 5,657,046 (hereinafter referred to as "Noble"). Applicant respectfully traverses and submits that in view of the amended claim 21, this rejection is no longer proper. Therefore withdrawal of the present rejection is respectfully requested.

Rejection of claims 21 and 2-11 under 35 U.S.C. §102(b)

Claims 21 and 2-11 stands rejected under 35 U.S.C. §102(b) as being anticipated by Kehlet et al., U.S. Patent No. 5,956,046 ("Kehlet"). Applicant respectfully traverses.

As understood, Kehlet is directed to, *inter alia*, a scene synchronization for multiple computer displays (20A-20C). Kehlet discloses, *inter alia*, a system having three separate and distinct graphics accelerators (40A-40C) which communicate via a drawing signal 102 for providing graphics outputs (30A-30C) to the video monitors (20A-20C). In the preferred embodiments, the graphics accelerators 40 receive a reference synchronization signal 110 to provide for synchronization therein. As disclosed in Kehlet, "the drawing signal 102 is used to

communicate the collective state of each graphics accelerator 40 relative to an impeding scene switch." (*See*, col. 5, lines 32-34). Furthermore, FIG. 3 illustrates a graphics accelerator, such as one of any graphics accelerator 40A-40C. The graphics accelerator 40 receives pixel data from the previous stages of the graphics pipeline which is provided to the frame buffer unit 210. Through the pixel multiplexor 220 and the DAC 230, the video signal 240 is generated, which is provided to the display device 20. As succinctly illustrated in FIG. 3 and the accompanying discussion on col. 5, line 39-col. 5, line53, each specific graphics accelerator is independently operated and independently produces video signal 240 from the display device 20 and provides interaction solely through the drawing signal 102. As discussed above, the drawing signal 102 allows for the indication of an impending scene switch, whereby all three separate video screens may be synchronized for a timely scene switch. Kehlet discloses a video graphics system having, *inter alia*, three separate and distinct graphics accelerators 40 interconnected through a drawing signal 102 for providing the synchronization of the operation of the separate graphics accelerator 40 with respect to video outputs 20. Kehlet discloses, *inter alia*, a single specific image for each display and does not disclose a combined view screen across all three images whereupon the multiple graphics accelerator would generate an overall image frame composed of three separate portions of the screen, but rather discloses, *inter alia*, separate video signals which are synchronized solely through the use of a field locking of the displays.

Regarding amended claim 21, Applicant respectfully submits that Kehlet fails to disclose all of the claimed limitations. Claim 21, as amended, includes limitations previously presented in claim 4, specifically the step of rendering at least a second portion of the first frame of video with a second VGA in response to a second control signal including "storing the at least second portion of the active decoded video in a first memory associated with the first VGA." Therefore, Applicant will address the Examiner's submitted position found on paragraph 11 on page 4 of the present Office Action discussing the limitation originally found in claim 4.

In support of the present rejection, the Examiner asserts that Kehlet discloses "storing the at least second portion of the active video in a first video memory associated with the first VGA." As being disclosed by element 210 in FIG. 3. Applicant respectfully traverses and submits that upon further inspection, the frame buffer unit 210 of FIG. 3 is illustrated as being disposed within the first graphics accelerator 40A, also illustrated in FIG. 2. FIG. 3 illustrates

the frame buffer unit 210 receiving two input signals to each of the frame buffer memory banks 202A and 202B "from previous stages in graphics pipeline such that output pixel data is provided to pixel select multiplexer 220 on pixel input bus 0 222A and pixel input bus 1 222B. The DAC 230 provides the select signal to the multiplexer 220 such that the proper output video signal 240 is generated. As further discussed on col. 5, lines 30-65, the graphics accelerator 40A of FIG. 3 further illustrates the graphics accelerators 40B and 40C of FIG. 2. Based on the disclosure of Kehlet and the accompanying figures, the accelerators 40A, 40B and 40C are flow based units providing for a graphics pipeline input put into the frame buffer unit 210 such that a signal is output on the cables 30A, 30B and 30C. As understood, the only communication between the accelerators 40 is from the drawing signal 102 which communicates the collective state of each accelerator 40 relative to an impending scene switch and does not contain any actual active decoded video. Therefore, Kehlet discloses a system that has a graphics accelerator receive a distinct frame of active video, such as illustrated in the FIG. 2, there are three separate frames of video each individually provided to one of the three accelerators 40A, 40B and 40C.

Therefore, Kehlet discloses a system in which there is a forward flow of data from the frame buffer unit 210 to the DAC 230. Claim 21, as amended, specifically and succinctly claims "storing the at least second portion of the active decoded video in a first memory associated with the first VGA." Therefore, using the Examiner's analogy regarding the teachings of Kehlet, the first video graphics adapter would be the graphics accelerator 40A and the first memory would be the frame buffer unit 210 within graphics accelerator 40A. Furthermore, the second VGA would be either the graphics accelerator 40B or graphics accelerator 40C having a separate and different frame buffer unit 210 disposed therein. As claimed, claim 21 recites limitations directed to rendering at least a second portion of the first frame of video at a second VGA and storing the at least second portion of the active decoded video in a first memory associated with the first VGA. Therefore, for the Examiner's assertion of Kehlet to disclose the claimed present invention, Kehlet would need a system which provides an output signal provided from the DAC 230 within either the graphics accelerator 40C or graphics accelerator 40B to be provided to the frame buffer unit 210 stored within the graphics accelerator 40A.

This structure is not provided and not disclosed in Kehlet. In contradistinction, Kehlet discloses the exact opposite system providing for only drawing signal 102 to be provided

between the accelerators 40A-40C and the rendered second portion of the active decoded video provided to either the monitors 20B or 20C from either the accelerators 40B or 40C across video cables 30B or 30C. Therefore, Kehlet teaches a completely different system having a one to one correlation between the generated or rendered video from each of the accelerators to the output display and generates a completely different result wherein each of the graphics accelerator is a self sustaining except for timing information provided from the drawing signal 102. Whereas, the claimed present invention includes limitations provided for storing the at least second portion of the active decoded video in a first memory associated with the first VGA. Therefore, Applicant submits that Kehlet fails to disclose all of the claimed limitations in claim 21, as amended. Reconsideration and withdrawal of the present rejection are respectfully requested.

Regarding claims 2 and 5-11, Applicant respectfully submits that these claims contain further patentable subject matter in view of Kehlet. It is submitted that these claims are allowable not merely as being dependent upon an allowable base claim. For example, claim 5 provides limitations to "reading the second portion of the active decoded video from the first video memory and storing the at least second portion of the active decoded video in a first video memory associated with the first VGA." As discussed above, the system of Kehlet teaches away from this exact limitation and does not provide for data communication between the frame buffer unit 310 within the different accelerators 41A, 41B and 41C, previously discussed as frame buffer units 210 with respect to FIG. 3. Therefore, as the system of Kehlet and the corresponding illustrated structure does not provide for any communication of active decoded video between the frame buffer units, the system does not disclose reading active decoded video from memory and thereupon storing the active decoded video in another memory associated with a different VGA or graphics accelerator. Therefore, it is respectfully submitted that these claims contain further patentable subject matter and withdrawal of the present rejection is respectfully requested.

Rejection of claim 13 under 35 U.S.C. §103(a)

Claim 13 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kehlet and further in view of Lumelsky, U.S. Patent No. 4,949,169 ("Lumelsky").

Applicant respectfully traverses and resubmits the above position offered with regard to claim 1. As discussed above, claim 21 includes limitations which are not disclosed by the teachings of Kehlet, therefore claim 13 would provide further patentable subject matter as the limitations discussed above have not been asserted to have been disclosed by Lumelsky. Therefore one of ordinary skill in the art would not have been motivated to combine these references because the combination thereof would not have produced the claimed present invention. Therefore, it is submitted that claim 13 is allowable as containing patentable subject matter in view of the prior art of record and not merely as being dependent upon an allowable base claim. As such, reconsideration and withdrawal of the present rejection is respectfully requested.

Rejection of claims 22 and 17-19 under 35 U.S.C. §103(a)

Claims 22 and 17-19 stand rejected 35 U.S.C. §103(a) as being unpatentable over Kehlet and further in view of Lauer et al., U.S. Patent No. 5,523,769 ("Lauer"). Applicant respectfully traverses and requests reconsideration.

Regarding claim 22, Applicant respectfully submits that claim 22, as amended, contains limitations not taught or suggested by either Kehlet or Lauer, either individually or in combination thereof. As discussed above with regard to claim 21, Kehlet discloses a system having a specific one to one ratio between the graphics accelerator 40 and the displays 20. Furthermore, while each of the graphics accelerator 40 includes a frame buffer unit 210 stored therein, Kehlet does not teach or suggest any structure wherein the various frame buffers within the different accelerators 40A, 40C provide any interconnectivity therebetween for providing video data thereacross. Moreover, the only communication between the multiple graphics accelerators is the drawing signal 102, as described above. Therefore, as claim 22 has been amended to include further limitations including storing the first frame of active video in a video memory associated with the first VGA and displaying at least a portion of the first frame of video at a second VGA, the system of Kehlet does not provide for the connectivity to have the first frame be within a first frame buffer unit 210 and also be displayed or have at least a portion be displayed at a second monitor. More specifically, with respect to FIGS. 2 and 3 of Kehlet, at

Applicant respectfully submits that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: 10/6/03

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US 092702560PP1

Creation date: 09-16-2004
Indexing Officer: JROMANI - JOHN ROMANI
Team: OIPEBackFileIndexing
Dossier: 09270256

Legal Date: 11-05-2003

No.	Doccode	Number of pages
1	CTAV	2

Total number of pages: 2

Remarks:

Order of re-scan issued on .....